WHAT IS CLAIMED IS:

1	1. A method of testing an integrated circuit comprising:				
2	receiving test output data from a circuit-under-test;				
3	delaying the test output data;				
4	comparing the test output data with the delayed test output data to generate a first				
5	compare signal;				
6	generating a control signal; and				
7	comparing the control signal to the first compare signal to generate a second				
8	compare signal.				
1	2. The method of claim 1 further comprising:				
2	if the second compare signal toggles from a first state to a second state while				
3	receiving the test output data; then				
4	providing a signal indicating an error; else				
5	providing a signal indicating no error.				
1	3. The method of claim 1 further comprising:				
2	changing the control signal such that the second compare signal toggles from the				
3	first state to the second state.				
1	4. The method of claim 1 further comprising:				
2	toggling the control signal when the test output data is expected to toggle.				
1	5. The method of claim 3 further comprising:				
2	after changing the control signal such that the second compare signal toggles from				
3	the first state to the second state;				
4	providing a signal indicating an error.				
1	6. The method of claim 1 further comprising:				
2	after receiving test output data from a circuit-under-test; and				
3	retiming the test output data to a clock signal, the clock signal comprising a				
4	plurality of clock cycles.				

I	7.	The method of claim 6 wherein the test output data is delayed one clock			
2	cycle.				
1	8.	The method of claim 1 wherein the delay is done using a flip-flop.			
1	9.	The method of claim 1 wherein the test output data and the delayed test			
2	output data are reti	med to a clock signal, the clock signal comprising a plurality of clock cycles.			
1	10.	The method of claim 9 wherein the retiming circuits are preloaded with			
2	expected data to generate a first compare signal.				
1	11.	The method of claim 8 wherein the comparing the test output data with the			
2	delayed test output data to generate a first compare signal and comparing the control signal to the				
3	first compare signal to generate a second compare signal are done using a first exclusive-OR gate				
4	and a second exclusive-OR gate.				
1	12.	An integrated circuit comprising:			
2	a de	lay circuit;			
3	a fii	a first compare circuit coupled to the delay circuit; and			
4	a se	a second compare circuit coupled to the first compare circuit and further coupled			
5	to receive a control signal.				
1	13.	The integrated circuit of claim 12 further comprising:			
2					
2	a re	timing circuit coupled to the delay circuit.			
1	14.	The integrated circuit of claim 13 further comprising:			
2	a sta	ate machine coupled to the second compare circuit.			
1	15.	The integrated circuit of claim 12 wherein the first compare circuit and the			
2	second compare circuit are exclusive-OR gates.				
1	16.	The integrated circuit of claim 12 wherein the integrated circuit is a field			
2	programmable logi	c device further comprising:			

3		a plur	ality of logic elements coupled by a plurality of programmable interconnect			
4	lines.					
1		17.	The integrated circuit of claim 16 further comprising:			
2		an erre	or memory circuit coupled to the second compare circuit.			
1		18.	An integrated circuit comprising:			
2		a serie	es combination including a retiming circuit in series with a delay circuit,			
3	wherein the		etiming circuit is configured to retime test data to a clock signal and the delay			
4		onfigured to delay the test data;				
5	•	a first compare circuit coupled to receive an output of the series combination;				
6		a second compare circuit coupled to receive an output of the first compare circuit				
7	and further coupled to receive a control signal.					
1	•	19.	The integrated circuit of claim 18 wherein the delay circuit has an input			
2	coupled to a	n output of the retiming circuit.				
1		20.	The integrated circuit of claim 18 wherein a state machine is configured to			
2	provide the	control si	ontrol signal.			
1		21.	The integrated circuit of claim 20 further comprising a second retiming			
2	circuit configured to retime the test data and provide an output to the first compare circuit.					
1		22.	The integrated circuit of claim 18wherein the first compare circuit and the			
2.	second compare circuit are exclusive-OR gates.					
1	·	23.	The integrated circuit of claim 18 wherein the integrated circuit is a field			
2	programmab	able logic device further comprising:				
3		a plurality of logic elements coupled by a plurality of programmable interconnect				
4	lines.					
1		24.	The integrated circuit of claim 18 wherein the error circuit comprises an			
2	OR gate hav	ring an ou	atput coupled to an input of a flip-flop, the OR gate configured to receive an			
3	output from the flip-flop and the output from the second compare circuit.					

- The integrated circuit of claim 24 further comprising:
- a error circuit coupled to receive an output of the second compare circuit.

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